FETs come in several flavors. Look first at an n-channel depletion mode junction FET

\[ \text{(JET)} \quad \begin{array}{c}
\text{G}
\hline
\text{source, gate, drain}
\end{array} \]

\[\begin{array}{c}
\text{D}
\hline
\text{n}
\end{array} \]

1) → Conductor.

IF \( V_G = 0 \), get limited conduction depending on \( V_{DS} \).

IF \( V_G < 0 \),

(no gate current!)

\[ Z_n \rightarrow \infty ! \]

\[ \text{depleted region -- e- are driven away.} \]

IF \( V_{DS} \) small, effect is to vary resistance \( R_{DS} \) with \( V_G \).

IF \( V_{DS} \) large (\( \approx \) few \( V \)), get complete depletion \( \rightarrow I_{DS} \) is limited to a value determined by \( V_G \) (good for amplifier use).

So we need two types of plots:

1) Look at \( I_D \ vs \ V_G \) for a fixed \( V_{DS} \) ---

\[ \text{\( I_{PSS} \) = current for \( V_G = 0 \)} \]

(or "\( V_{GS\ (off)} \))

\[ \text{\( V_G \) can't exceed \( \pm 5 \) \( V \) or \( \approx \) 6 conduct!} \]

(\text{Note semi-log scale.})

2) Look at \( I_D \ vs \ V_{DS} \) for various \( V_G \)

\[ \text{\( I_{DS} \) \& \( V_G \) \( \propto \) \( V_{DS} \)} \]

\[ \text{\( I_{DS} \) \& \( V_G \) \( \propto \) \( V_{DS} \)} \]

\[ I_{DS} \propto \begin{cases} \text{V}_{GS} & \text{for} \text{ V}_{GS} > 0 \\ \text{R} \propto \text{V}_{GS} & \text{for} \text{ V}_{GS} < 0 \end{cases} \]

\[ I_{DS} \propto (\text{V}_{GS} - \text{V}_T)^2 \]
Saturation occurs when deflection blocks the channel completely. So we can use device either as a variable resistor, $V_r$ or $V_t$ for each mode.

$$I_D = \frac{2k}{2} \left( (V_{GS} - V_P) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad \text{(low $V_{DS}$)}$$

$$I_D = k (V_{GS} - V_P)^2 \quad \text{(saturation)}$$

Finally, for very small $I_D (< 1mA)$, $I_D = k (V_{GS} - V_P)$

Simple current source:

\[ +V \]
\[ Q \]
\[ R_c \]
\[ \times \]
\[ L \]
\[ \times \]

Operate in sat. region. Then

$$I_L = I_{DSS} \text{ approximately (} \approx k V_P^2 \text{)} \quad \text{set by device.}$$

To vary, use "self-biasing."

Since $I_G = 0$, quite accurately,

$$V_{GS} = 0 \quad \text{hence} \quad I_S = I_D.$$ 

Also $V_{GS} = I_s R = -I_D R$

So we have a (-) bias.

Current will be $I_D = k (I_D R - V_P)$

(Still independent of $V_{DS}$)

$$I_D = \frac{1}{kR}$$

Transconductance --

Most commonly, amplifiers are designed using $g_m = \frac{I_D}{V_{GS}}$ to change in drain current.

Measured in "mhos".

It's smaller than for junction transistors

$$g_m \approx 2V_{TH}$$

$\Rightarrow$ High input $Z$ is main FET virtue.
One common use is \textit{FET} input circuit ---

\begin{center}
\begin{tikzpicture}
  \node (input) at (0,0) {$V_g$};
  \node (source) at (1,0) {$V_s$};
  \node (load) at (2,0) {$R_L$};
  \node (output) at (3,0) {$V_D$};
  \draw (input) -- (source);
  \draw (source) -- (load);
  \draw (load) -- (output);
\end{tikzpicture}
\end{center}

--- \textit{source follower} ---

\( V_s = g_m R_L / \text{since} \quad I_s = I_D \)

\text{Using} \quad I_D = g_m V_g = g_m \left( V_g - V_T \right) \quad \Rightarrow \\
\( V_s = \left( \frac{R_L g_m}{1 + R_L g_m} \right) V_g \quad \text{(but note that)} \quad g_m \approx \frac{2 V TD}{g_m} \text{depends on operating point!} \)

\( \approx V_g \quad \text{if} \quad R_L g_m \gg 1 \)

\text{Output impedance is} \quad \frac{1}{g_m} \quad \text{like emitter follower,}

\text{but less impressive (\approx \ 100 \ \Omega)}, \text{However, } Z_{in}

\text{is very large, especially with MOSFETS.}

Another common use is \textit{variable resistor}.

\begin{align*}
\text{When} \quad \text{applies} & \quad \Rightarrow \\
\frac{I_D}{V_{DS}} &= \frac{1}{R_{eff}} = 2K \left( (V_{GS} - V_T) - \frac{V_{DS}}{2} \right)
\end{align*}

\text{Usable values --- few \ 2 \ to \ 8.}

\text{Suggest use for: modulation, gain control, analog switch}

\text{But usually we use MOSFETS for this ---}
**Typical MOSFET:**

![MOSFET Diagram](image)

(NMOS)

**Enhancement mode:** make gate (+) to create an n-type channel for conduction.

**Depletion mode:** vary doping so a (-) voltage discourages conduction. (Fairly rare)

\[
\log \frac{I_D}{I_D^0} \quad \leftarrow \quad \text{OK to bias gate (+)}
\]

\begin{align*}
V_T & \quad \text{depletion} \quad \text{JFET} \quad \text{enhancement} \\
-4 & \quad -3 \quad -2 \quad -1 \quad 1 \quad 2 \quad 3 \quad V_{GS}
\end{align*}

**P-channel:** mirror image.

So, we usually use MOSFET’s as switches.

- no gate leakage (but there is capacitance!)
- 0V is "off"

**Symbols:**

\[
\begin{align*}
\text{J} & \quad \text{body} \\
\text{G} & \quad \text{s} \\
\text{n-channel} & \\
\text{p-channel}
\end{align*}
\]

Body usually connected to ground, in power MOSFETs.
Typical switch -- analog:

\[ \begin{align*}
\text{signal in} & \quad \downarrow \\
+15V \quad \text{on} & \quad \uparrow \\
\text{off} & \quad \downarrow \\
\text{out} & \quad \uparrow \\
\text{large enough to avoid saturation}
\end{align*} \]

\[ RDS \text{ varies from } \sim 10^{10} \Omega \]
\[ \text{to } 25 - 100 \Omega \]

Can be used for multiplexer, reset, etc.

Nice integrated switches available.

Logic & power switching: common-source inverter

\[ \text{For power designs, can have } R_{\text{on}} \sim 0.01 \Omega \]!!

Good for driving loads.
Better is

![CMOS inverter diagram]

Input grounded --

\[ V_{gs1} = 0 \quad \text{(off)} \]
\[ V_{gs2} = -15 \, V \quad \text{(on)} \]

Basis of logic chips

Power FETs -- size with big gates (high \( C \), low \( R_{on} \))
- Can have on-state \( R \) of \( < 0.005 \, \Omega \)
- Currents up to \( > 100 \, A \)
- Voltages \( > 1000 \, V \)
- Thermally stable -- can use in \( H \)

But,
1) Large capacitance -- high gate currents needed to switch rapidly
2) Static - sensitive
3) Easily damaged by reverse gate bias outside specs
4) Need \( > 10 \, V \) to fully switch on, in some cases
5) Body connected to source -- forms a diode:
   \[ G \]